Impact of On-Chip Multi-Layered Inductor on Signal and Power Integrity of Underlying Power-Ground Net

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Agenda

- Background and motivation
- Simulation setup
- Simulation results
- Conclusion and future work

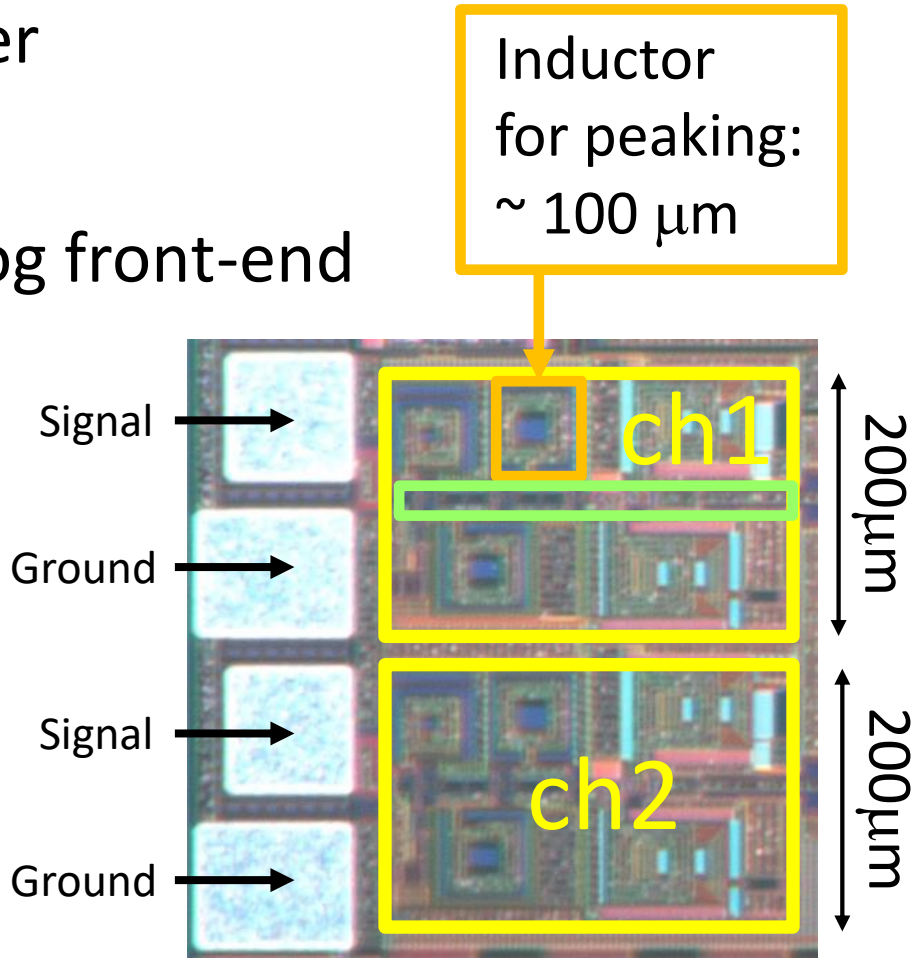
Background

Parallel, high-density optical interconnect for high speed data transfer

Demand on small area analog front-end

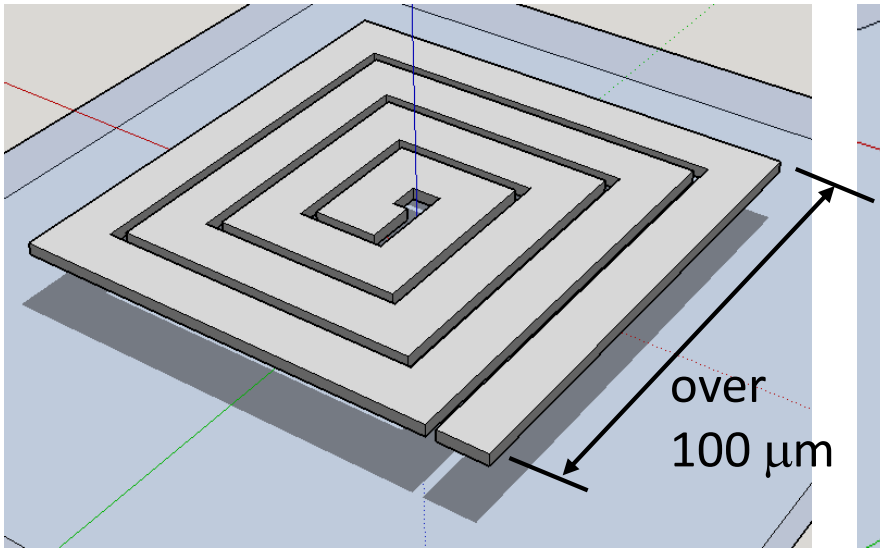
Inductors needed for bandwidth enhancement

Huge area occupied by inductors



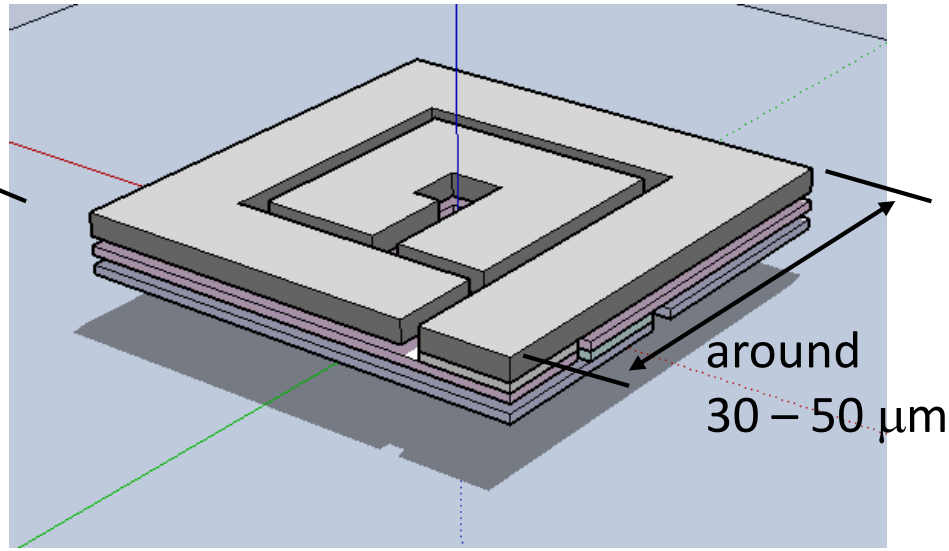
Small Area Inductor

Spiral Inductor



- ✓ Top (Thick) metal only
- ✓ High Q-factor
- ✓ Huge area

Solenoid Inductor

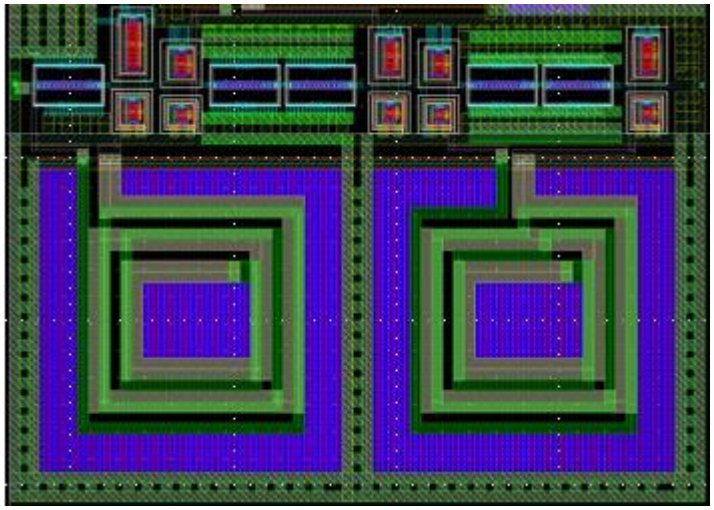


- ✓ Use lower layers
- ✓ Low Q-factor
- ✓ Small area

Solenoid inductor is effective for inductive peaking

More Area-Saving

Is it OK to stack inductor on circuits?



Solenoid is smaller,
but still needs >50μm□

Nothing under inductor

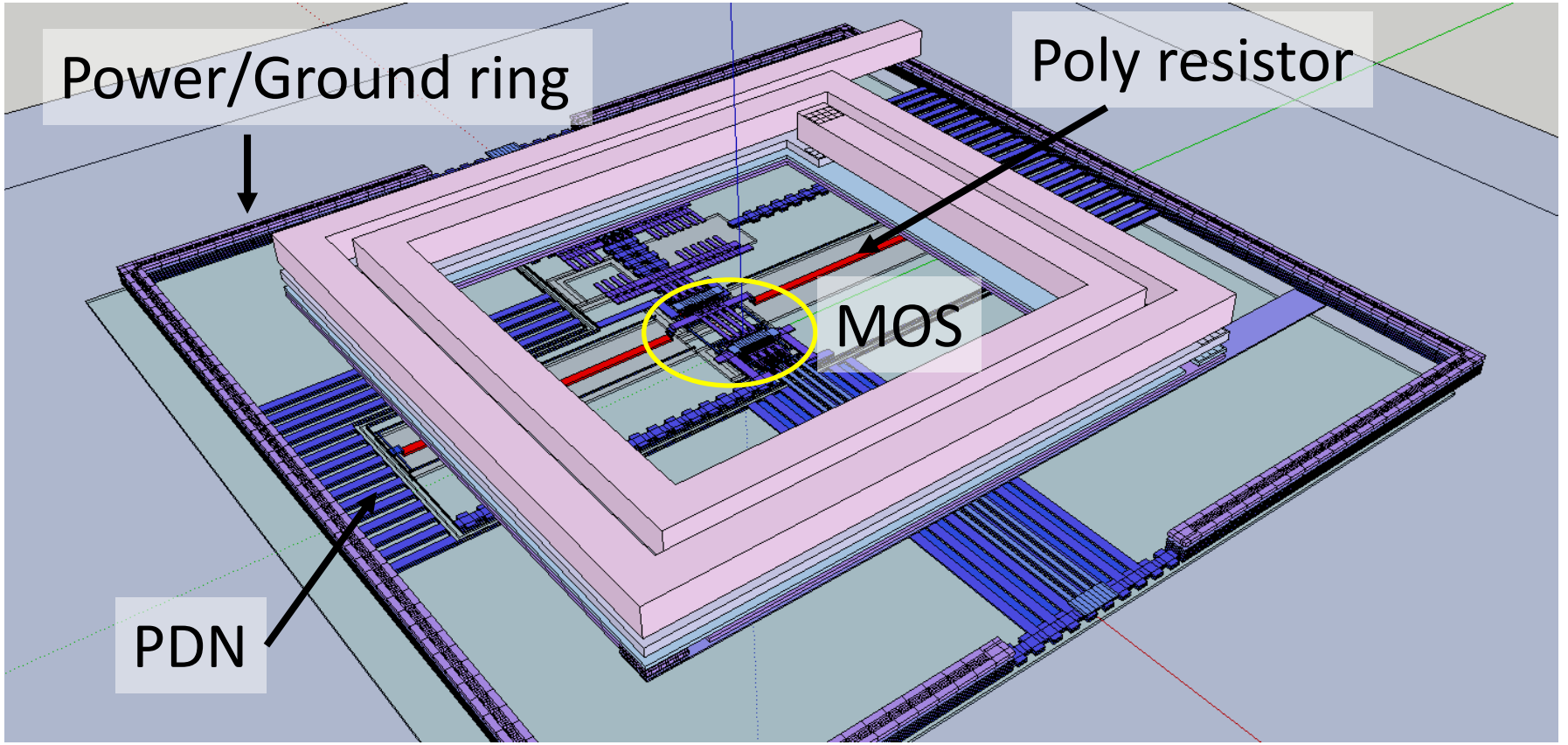
- ✓ Modeling accuracy
- ✓ Prevent coupling

If stacking is OK, we can save area more

Aim of this paper:

Investigating coupling between inductor and PDN

Stacking Inductor on Circuit



Largest facing area to inductor is PDN (power delivery network)

How should we design PDN under inductor?

Agenda

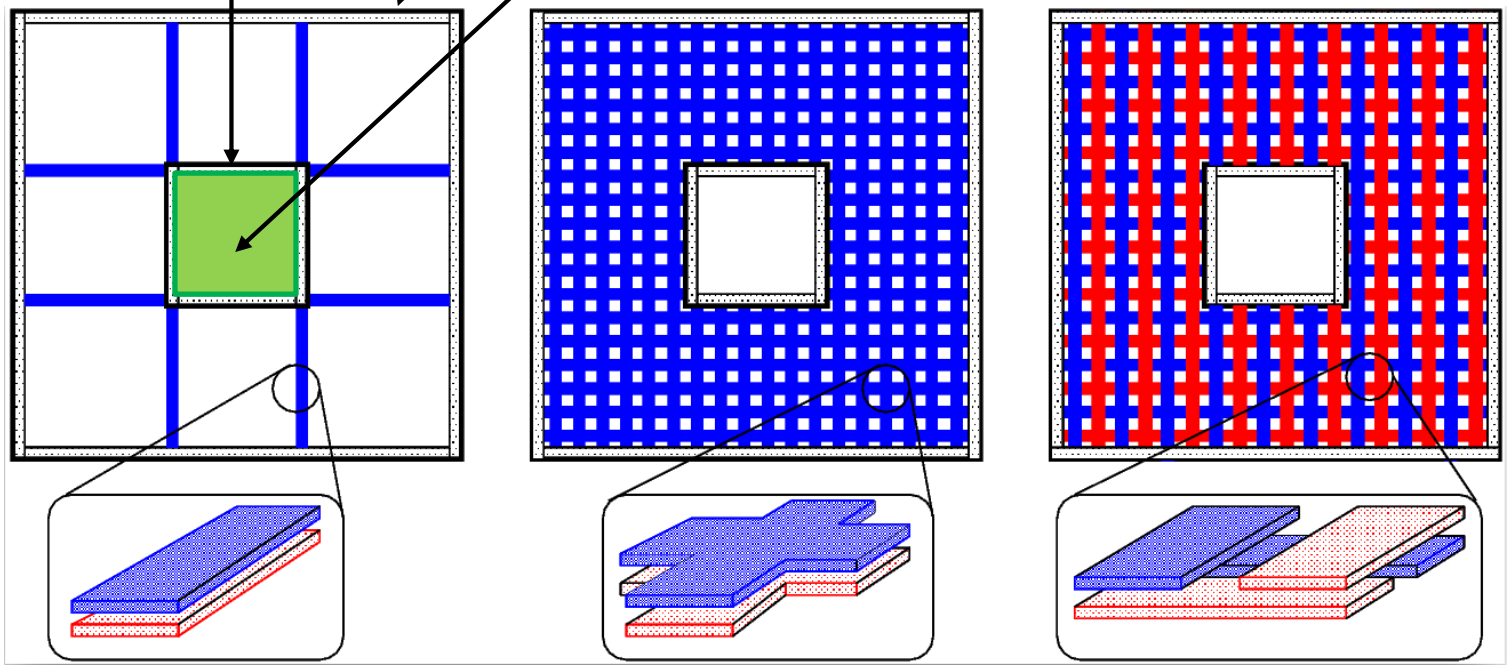
- Background and motivation
- Simulation setup
  - Power/Ground network structure
  - Structure of inductor
- Simulation results
- Conclusion and future work

Power/Ground Structure

Inner ring:
Circuit's P/G

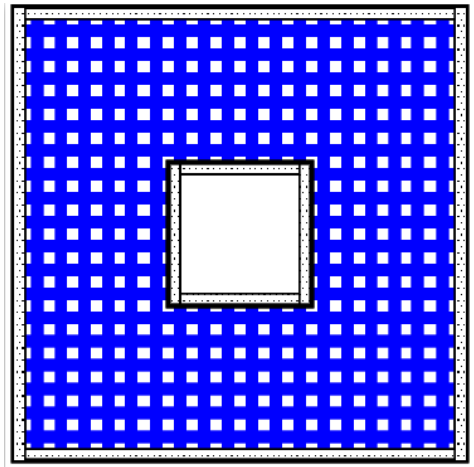
Outer ring: Ideal P/G

Core: Area for circuit (amplifier)

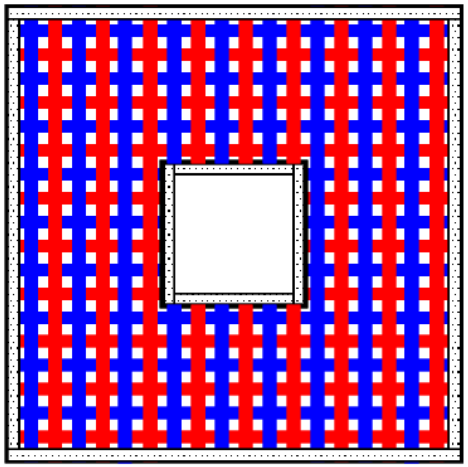


(a) Sparse (b) Mesh (c) Woven

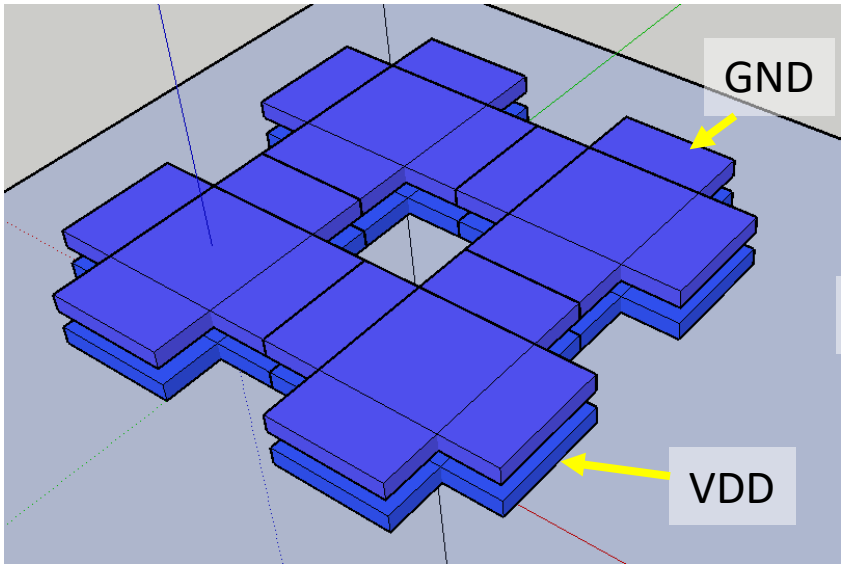
3D Image of Mesh and Woven



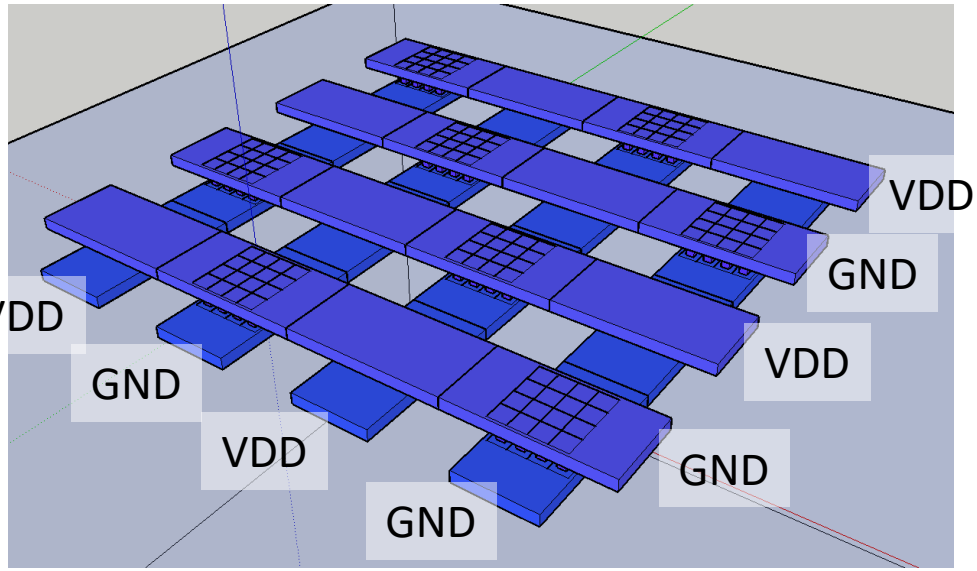
(b) Mesh



(c) Woven

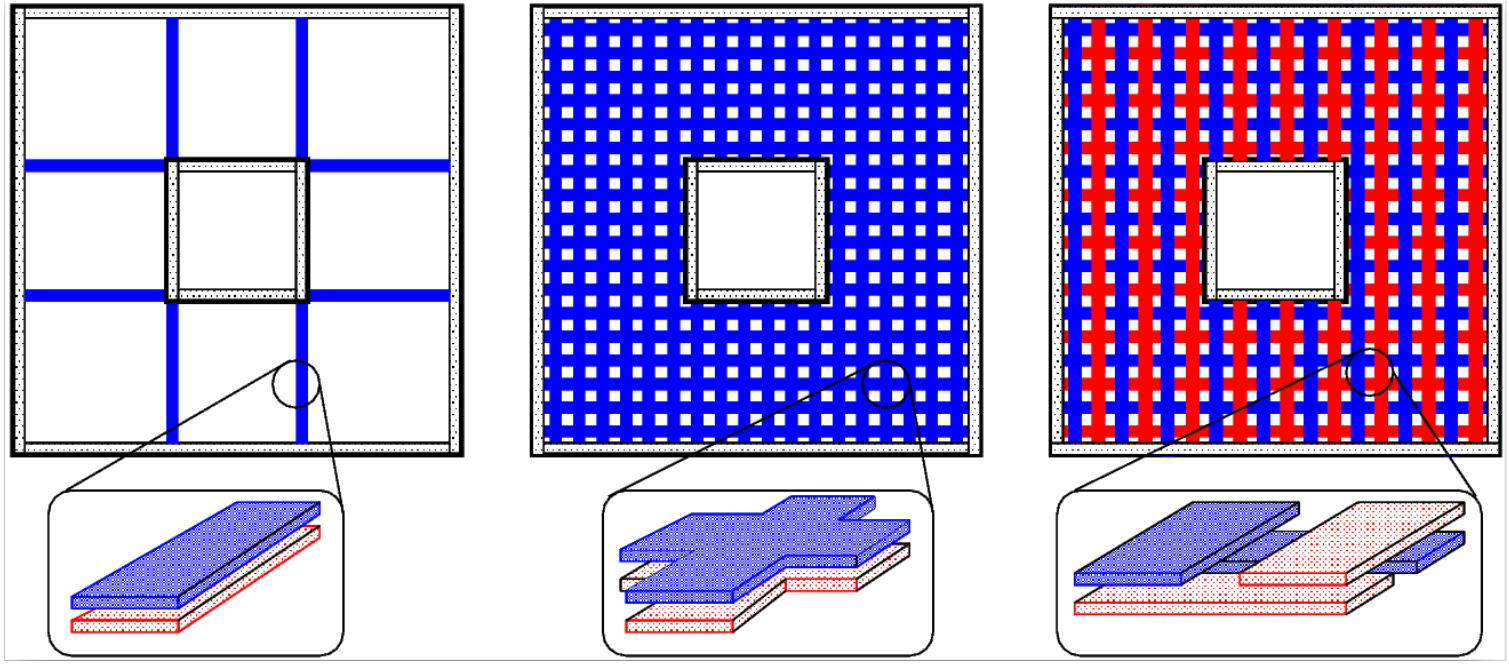


Mesh structure



Woven structure

Comparison



(a) Sparse

Minimize C coupling

Small decoupling

(b) Mesh

M2 (GND) couples stronger

Large decoupling

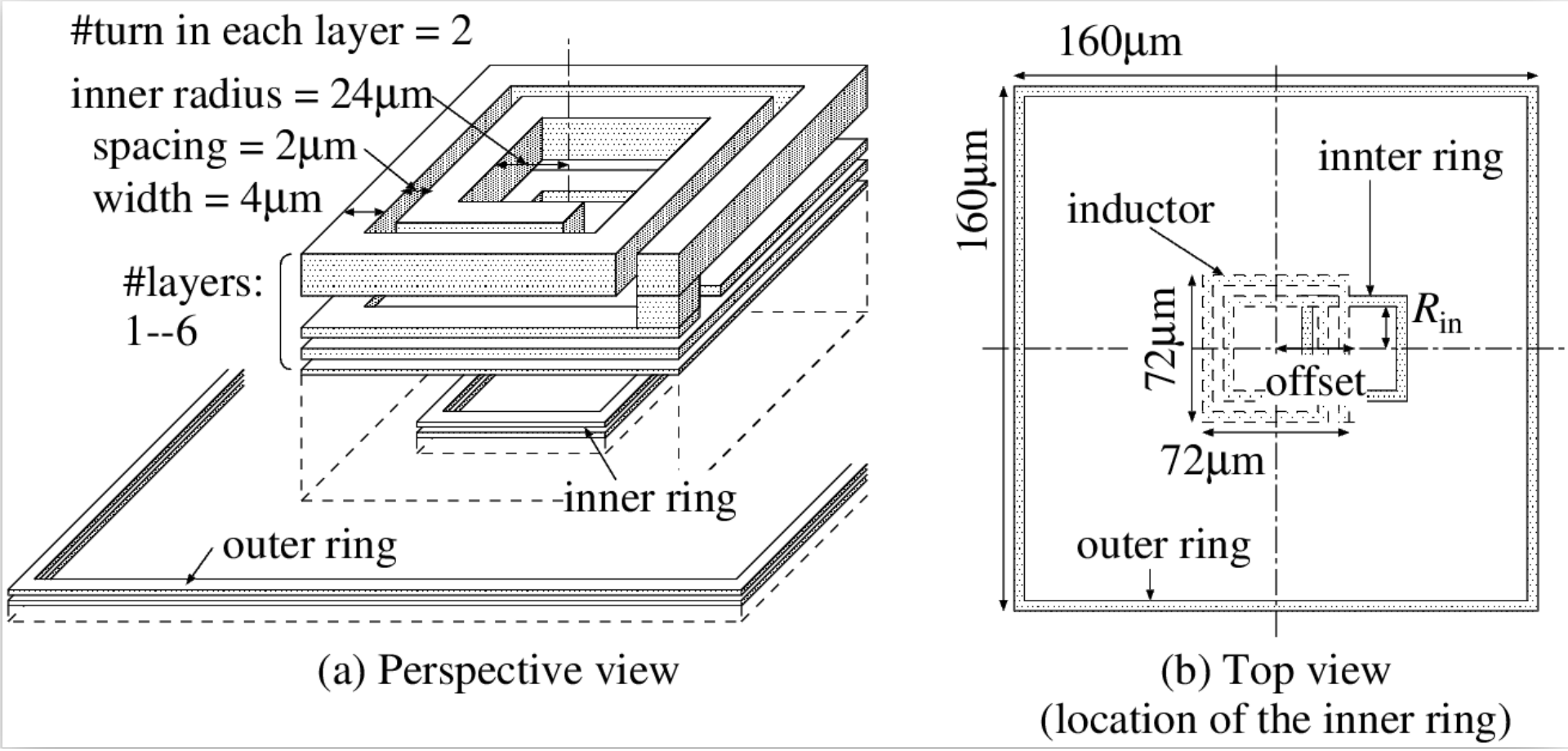
(c) Woven

Couplings are balanced

Large decoupling

* decoupling: decoupling capacitance between Vdd and GND

Parameters



# of layers of inductor

Size and position of inner ring (core area)

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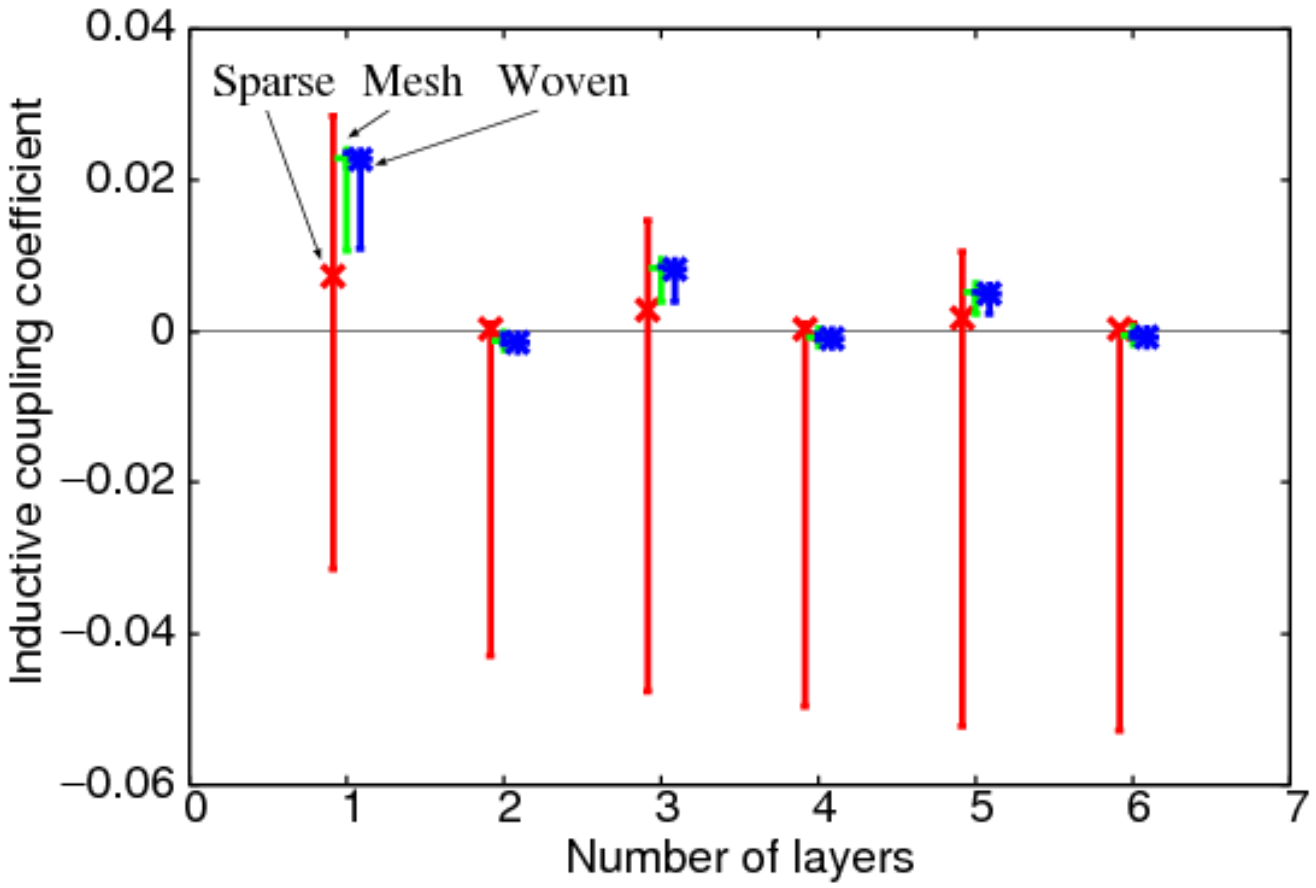
- Background and motivation
- Simulation setup
- Simulation results
  - Evaluation in inductance/capacitance value
  - Evaluation in transient analysis
- Conclusion and future work

Inductive Coupling (Coupling Coeff.)



Coupling coeff.:

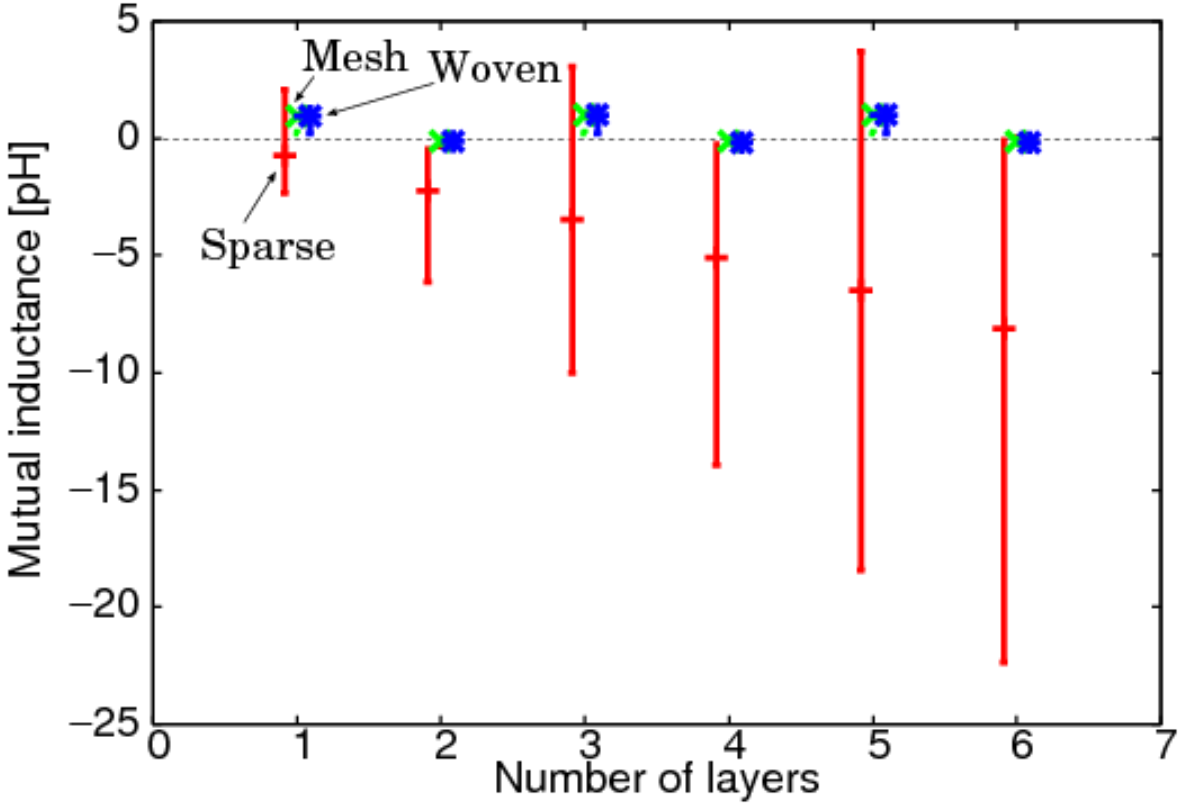
$$k = \frac{M}{\sqrt{L_1 L_2}}$$

* dot: zero offset of inner-ring
* Error-bar: effect of offset of inner ring

Increasing #layers = inductor get closer to PDN, but

In Mesh and Woven, coupling coeff. decreases

Inductive Coupling (Mutual Inductance)



$$k = \frac{M}{\sqrt{L_1 L_2}}$$

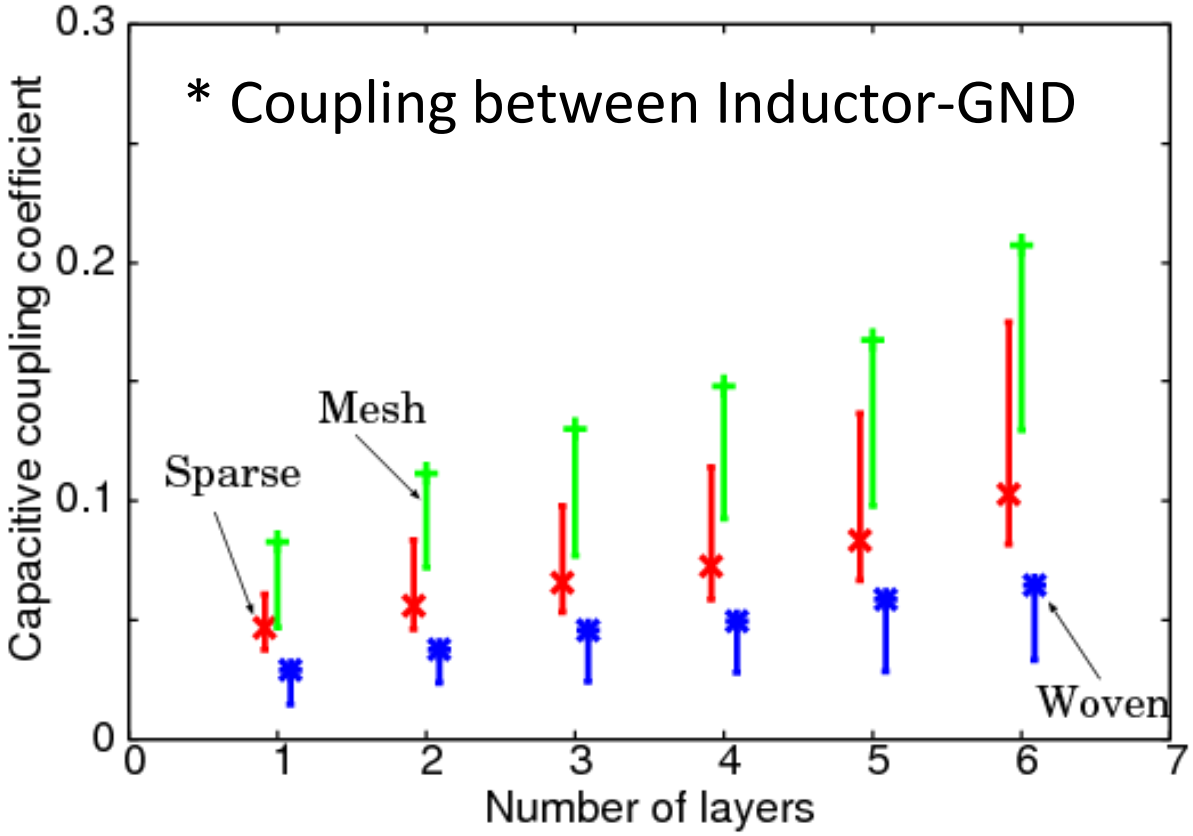
In Mesh and Woven,
L of PDN is small

Small coupling coefficient

Dense PDN can make inductive coupling almost zero even #layer increases

Capacitive Coupling (Coupling Coeff.)

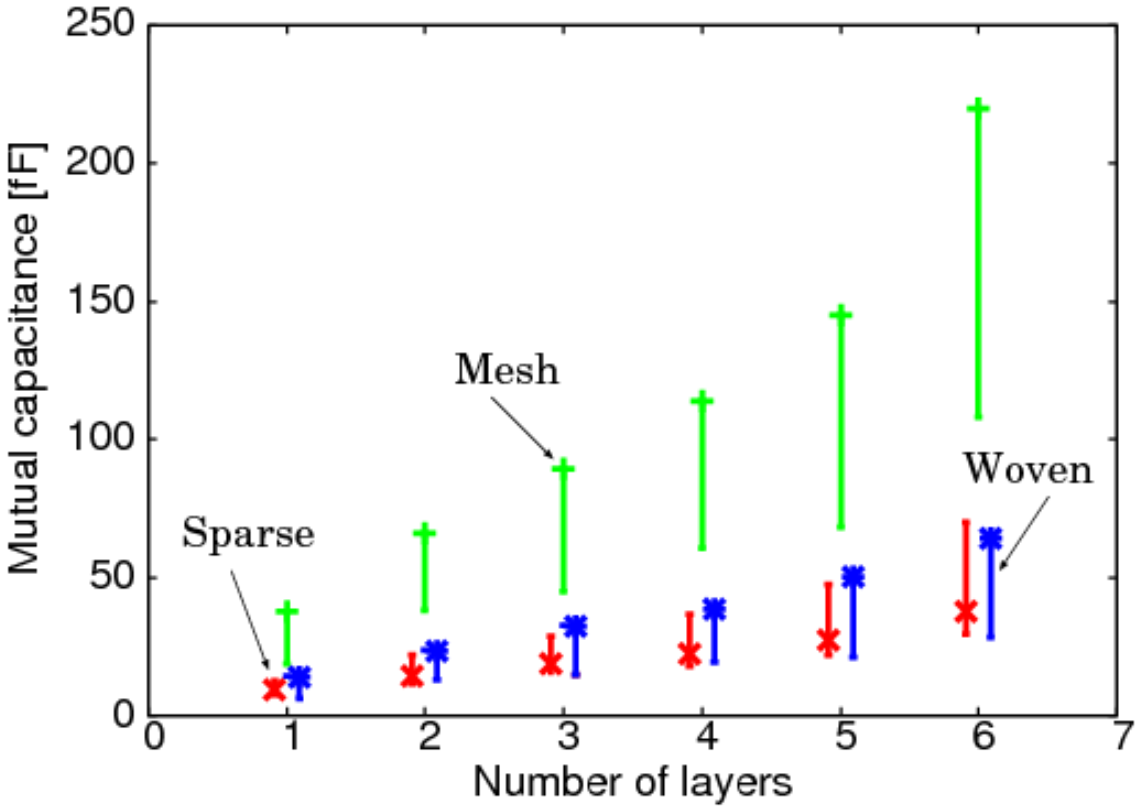
Much larger than inductive coupling coefficient (< 0.05)



Note:
Coupling of Mesh is largest, but Inductor-Vdd coupling of Mesh is almost zero

Sparse structure has larger coupling

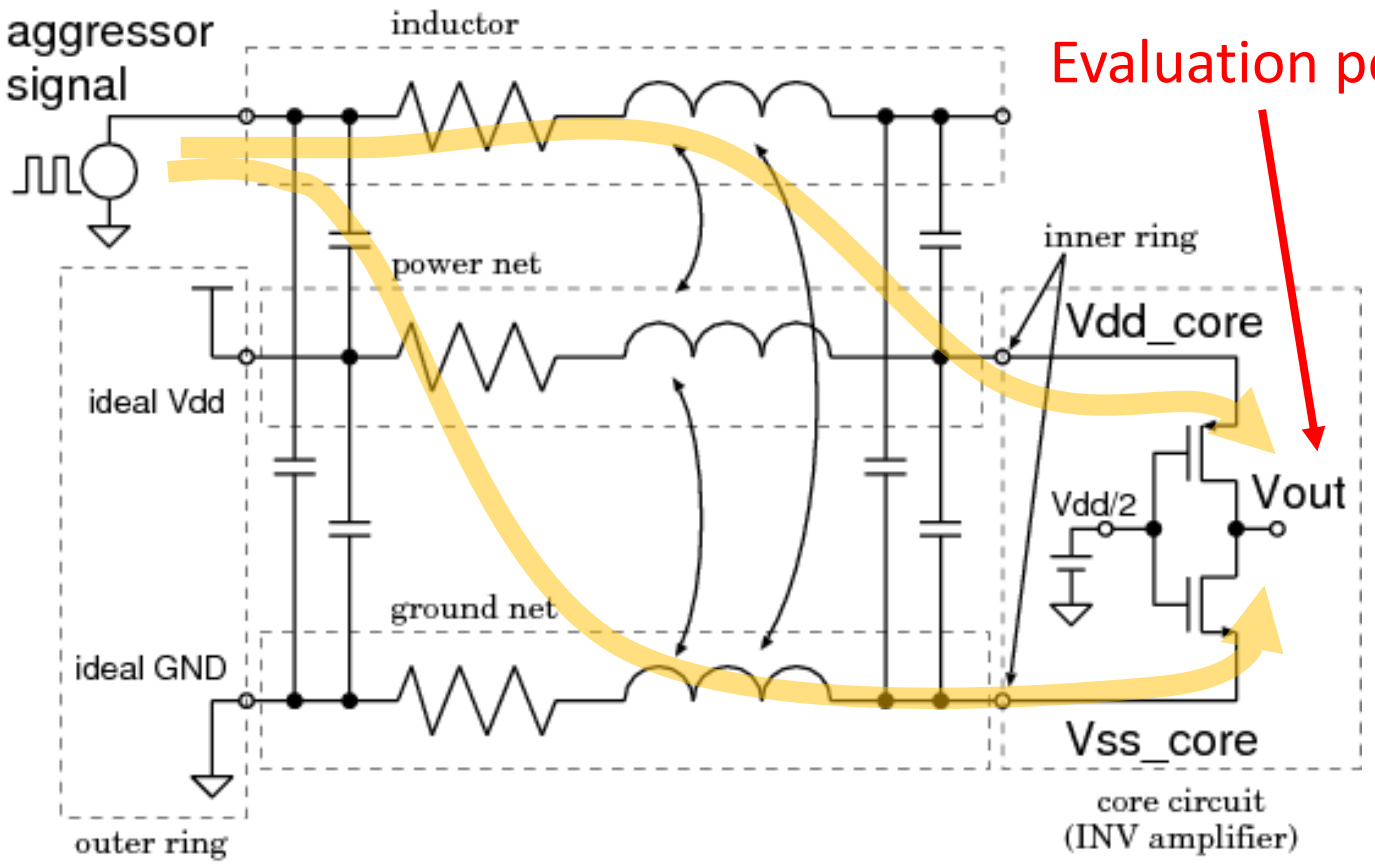
Capacitive Coupling (Coupling Capacitance)



Sparse is small or comparable to Woven,
but Woven has larger Vdd-GND capacitance
-> Coupling coefficient of Sparse becomes larger

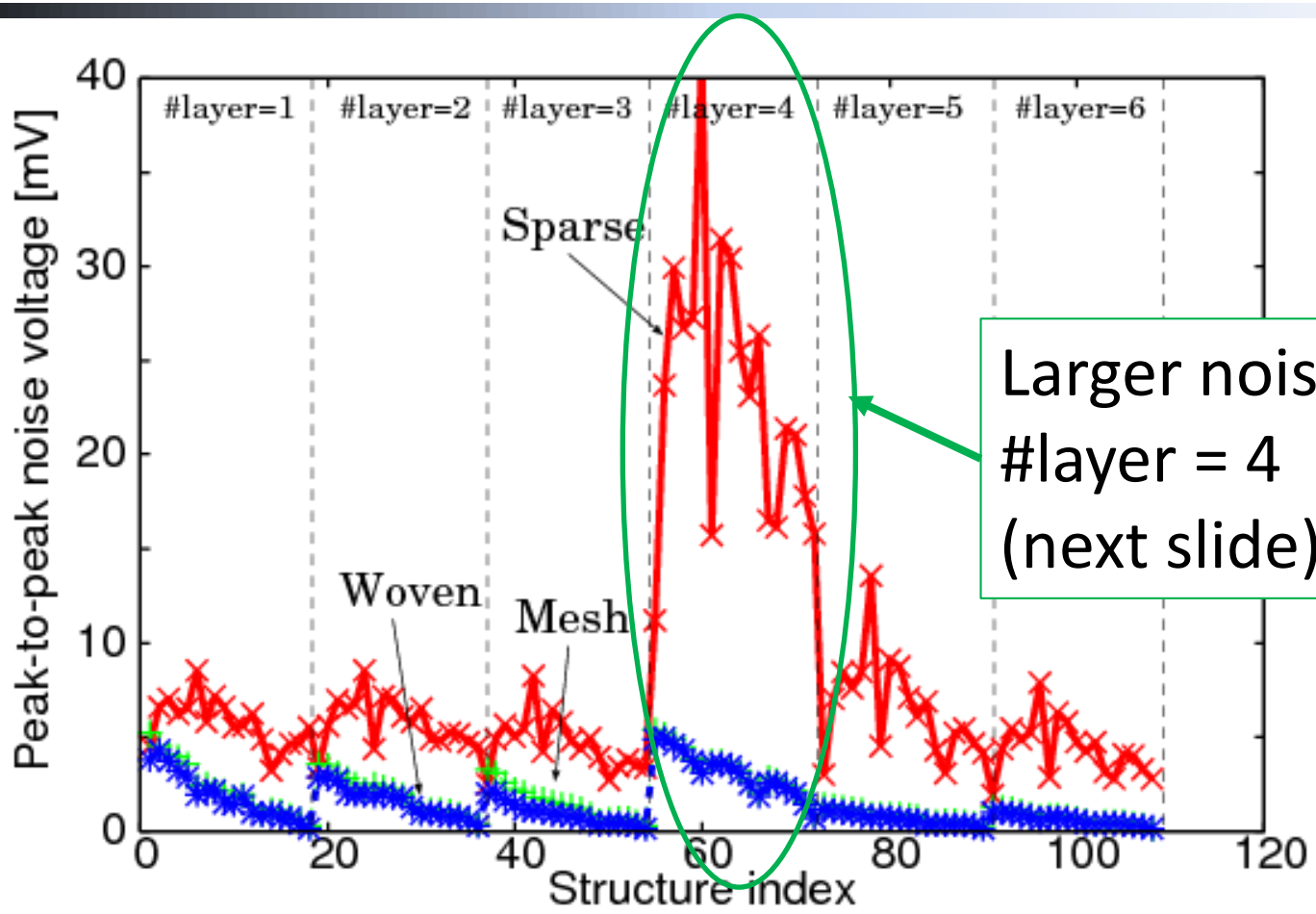
Transient Analysis on SPICE

Periodic pulse
50ps pulse width
20ps rise/fall time
(20Gbps signaling)



Coupled π-model for power/ground/inductor network

Noise Peak-to-peak Voltage



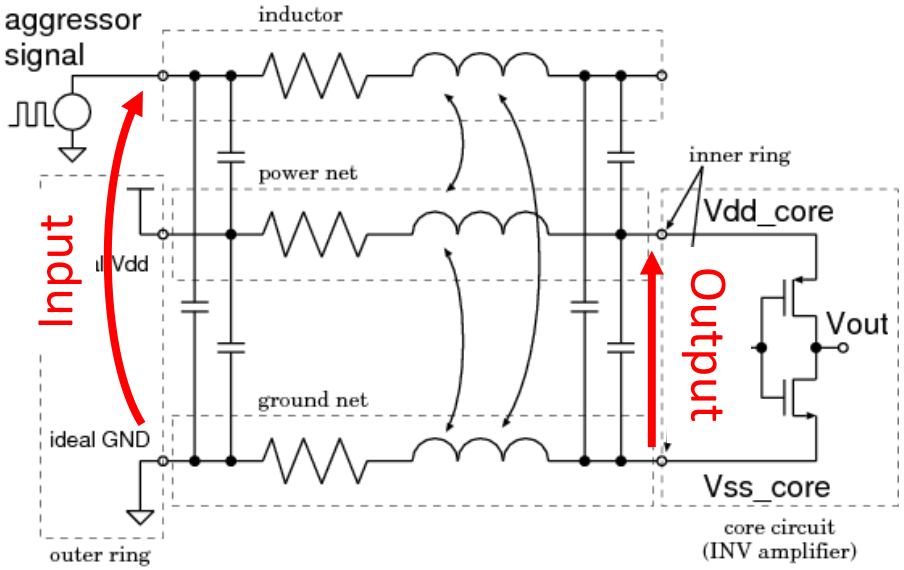
Larger noise when #layer = 4 (next slide)

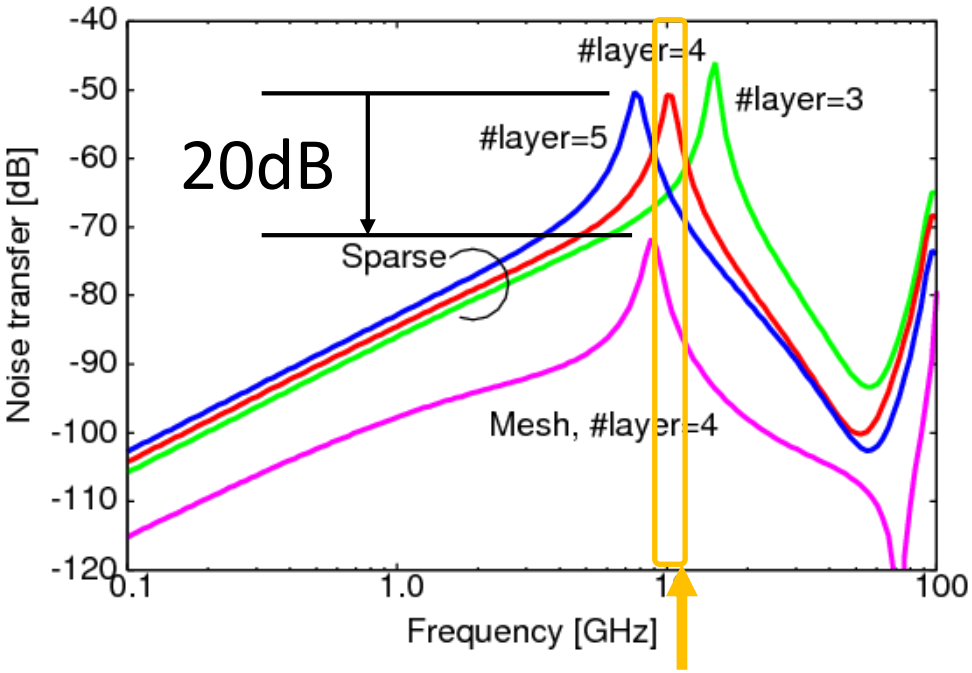
Sparse causes larger noise

Difference between Mesh and Woven are small

Impact of Resonance

Noise transfer function from aggressor to inner ring

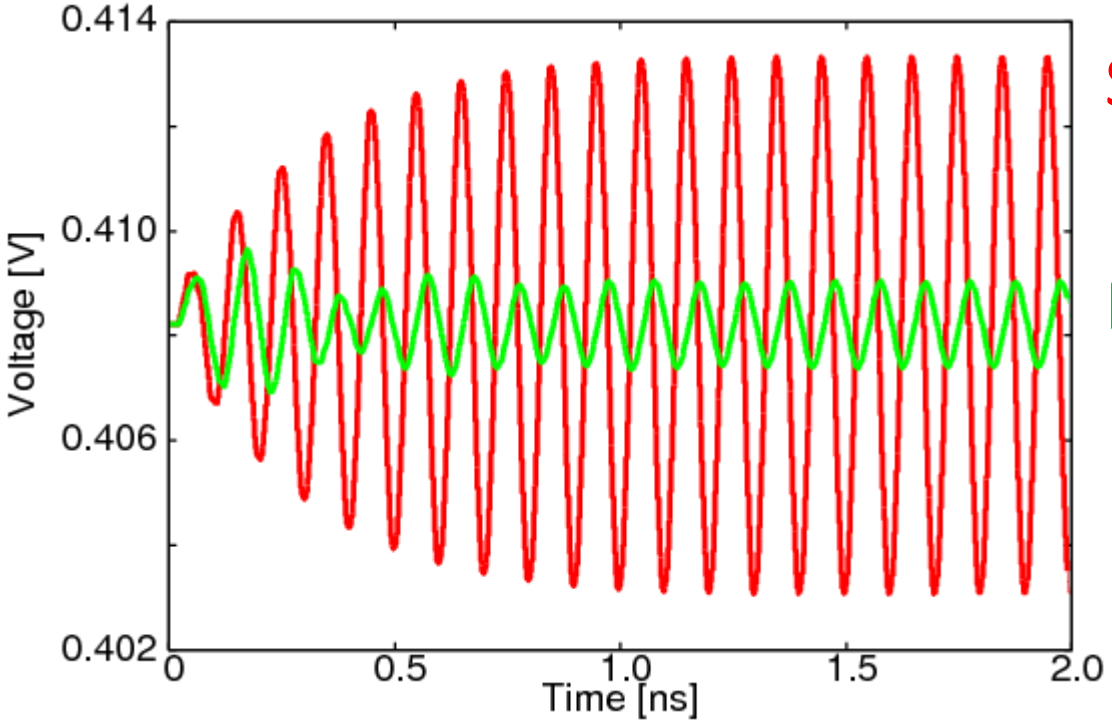




Aggressor input is 20Gbps = 10GHz clock

Mesh also has resonant frequency near 10 GHz, but transfer function is 20dB smaller

Noise Waveform



Sparse, #layer = 4

Mesh, #layer=4

Resonance make noise larger

Mesh and Woven can reduce impact of resonance

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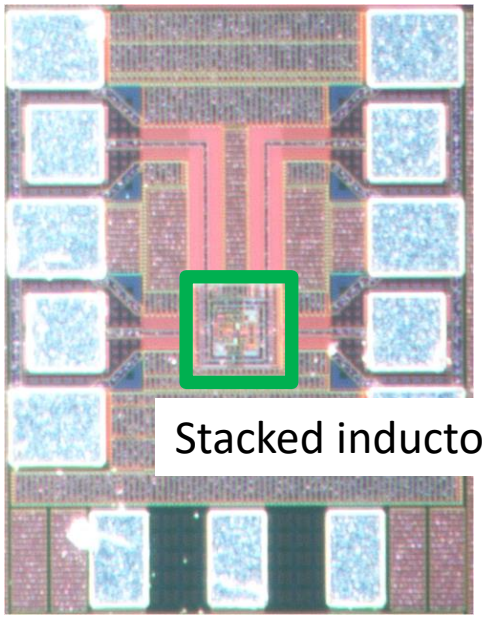
Summary

- Coupling of inductor and PDN is investigated
  - Stacking Inductor on circuit
  - Test 3 structures: Sparse, Mesh, Woven
- PDN should have dense P/G wires
  - Even inductor get closer, Mesh and Woven are better than Sparse
  - Sparse has a risk of large noise due to resonance
  - Dense structure (Mesh and Woven) can suppress the impact of resonance

Future Work

Remaining questions:

- Coupling to substrate is not discussed
  - Mesh/Woven might shield coupling to substrate
- Is lumped model adequate?



Stacked inductor/amp.

Chip fabrication is completed

Now we are preparing
real chip measurement