Power Integrity of Networking Processor at System Level

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Introduction

- The power density for high performance silicon devices such as networking processors is increasing with the feature size reduction of the transistor and the relative power dissipation of the interconnect in the currently deployed 16nm and below FinFet process nodes.

- Higher power, higher di/dt and heterogeneous integration of multiple silicon components in a single package further increases the power distribution challenge.

- The power integrity (PI) of networking processor at system level has to face several challenges…
The power integrity challenges for networking processors:

- the understanding of the device behavior in the networking processor application context,
- the efficient modeling for power integrity analysis,
- the importance of system level abstraction,
- the expected outcome of a power integrity analysis, illustrated by examples.
What is Power Integrity (PI)?

- Power Integrity (PI) means to ensure that the supply of a device is meeting the specification & requirements by using models and simulation of the Power Delivery Network (PDN).

- PI should answer to the following questions:
  - Is the supply network aligned with requirements?
  - Is the PDN impedance profile compliant with the application?
    - A PDN impedance reduction in the critical frequency ranges
    - An efficient & optimized placement, number and value of decoupling capacitors
  - Is the voltage at transistor level within the specified range?
    - A voltage noise reduction at transistor level (margin)

- Benefits:
  - Full system analysis in the various environments (IC, package, board),
  - Secures performances, optimize Build Of Material (BOM).
What is a Networking Processor?

- A device integrating several high speed serial link interfaces (SERDES @ 56Gbps +), processing units (~GHz and ~100W+) and memories with search capabilities (TCAM).

- Performance increase, integration (multi billion transistors) and power consumption reduction are the main drivers for the development of networking processors.

- Using Thermally Enhanced Flip Chip Ball Grid Array packages (TE-FCBGA) based on multi-layer laminate substrates.
Device Behavior for Power Integrity
PI Contributors of a Networking Processor

- Processing unit
  - ARM CPU with different activity states: idle, max power, wait for interrupt, cache miss…
  - Dedicated processing unit with clock gating, power switches…
  - Clock frequency, interrupt occurrences
  - Placement in silicon device

- TCAM
  - Different modes: Search/Compare, Idle…
  - Mode change, frequency
  - Placement in silicon device

→ Contributes to huge di/dt (several A/ns) at various frequencies
PI Contributors of a Networking Processor

- SERDES interfaces (high speed serial links)
  - Interface setup: Lane count, data rate per lane & per interfaces, synchronous/asynchronous behavior, burst, idle…
  - Interface frequency, state changes
  - Placement in silicon device
- Package routing and decoupling capacitors
- Board routing and decoupling capacitors
- Voltage regulator
Processing Unit with TCAM

- Processing unit like an ARM CPU
  - Main frequency
  - Low voltage (0.8V)
  - Events: wait for Interrupt, max computing...
  - Event occurrences: depending on system
  - Modeling of different state/events

- TCAM
  - Main frequency
  - Low voltage (0.8V)
  - Events: Idle, Search/Compare...
  - Event occurrences: depending on network activity and location on device
  - Modeling of different state/events

- Main contributors to power integrity
- Multiple cases to consider depending on system activity
- Identifying the relevant worst cases for power integrity requires a really good understanding of networking processor behavior in the system.
• SERDES interface
  • Various data rate to consider simultaneously and/or asynchronously depending on interfaces
    • IEEE 802.3 / OIF-CEI-04.0: 1.25G NRZ, 10G NRZ, 25G NRZ Long Reach, 28G NRZ Medium Reach, 56G PAM4 Very Short Reach, 56G PAM4 Long Reach…
  • Events: idle, data transfer, burst…
  • Event occurrences: depending on system
  • Modeling of different state/events

➡️ Most challenging contributor to power integrity
➡️ Multiple cases or patterns to consider depending on system activity
➡️ Identifying the relevant worst cases for power integrity requires a really good understanding of serial link behavior in the system.
Modeling for Power Integrity
Modeling for Power Integrity

• Power integrity (PI) analysis requires use cases and targets
  • Time domain: functional use-case and voltage noise target
  • Frequency domain: impedance target or template

• Use-case and target definition: need a proper system understanding
  • IC specifications (frequency, voltage margin, current needs, operating points…) are sizing the system, but the knowledge of IC hardware and software architectures is key to enable PI analysis
  • ANSYS RedHawk can help to define use-cases using the dynamic vectorless approach, but user inputs are still required for result accuracy

• Chip Power Model (CPM): an interesting solution for system level analysis
  • Different content and accuracy depending on user input
    • Early CPM (static and perhaps dynamic) to start sizing the system
    • Static CPM for DC Irdrop, Dynamic CPM for system PI
    • Multiple or single ports, IC probing points, configurations…
    • Physical part (RLC) for impedance, Activity part (i(t)) for voltage noise
• Capturing the voltage budget available at die transistors based on power delivery network content
  • Voltage range at
    • voltage regulator (SMPS, LDO)
    • package balls
    • die bumps
    • transistors
  • Acceptable overshoot, undershoot, peak to peak noise and frequency range

• Requires a complete view of the system content
Available Modeling Approach: Silicon Device

• Using silicon device modeling tool enabling
  • a simple model (like ANSYS Chip Power model - CPM) based on a RC network of the power delivery network (PDN) on the die and several current sources,
  • a vector less, vector based (PRBS, VCD…), a use-case or single state/mode model,
  • only a few clock cycle behavior (ns).
  • based on die supply pin groups
  ➔ Good starting point but not enough for PI

• Need to build a model compliant with system level PI
  • Current profile duration (us, ms or more)
  • Capturing events (state changes, occurrences)
  • Scaling states
  ➔ Combining models is a major challenge to ensure reliable power integrity
Available Modeling Approach: Package & Board

- Using package/board modeling tool enabling
  - a simple RLCG model or S-parameter of the package & board based supply pin groups aligned with die pin groups
  - with connection for decoupling capacitor models, CPM, VRM

- Using available board models
  - RLCG model delivered by end customer of the networking processor

- Using decoupling capacitor models
  - RLC or S-parameter model delivered by SMD providers (Murata, TDK…)

- Using voltage regulator models
  - RLC or behavioral model (VRM) delivered by VR providers
Limitation of current approach

• Maturity of each model
• Available approach considers that the RC on die remains similar
• Die models are most of the time based on states or short events
• Pin groups are required to use the model in simulators
• Model mapping when die/package/board designs are at different stages/maturities
• Combined die models are required to enable a complete system PI (post processing of available models)
• Uncertainty on decoupling capacitor model compliance with system context: voltage, temperature, aging… ➔ De-rating required for accuracy but complex to put in place
Area of Improvement

• Enabling modeling in early stage of the silicon device design
  • Start from nothing but specification
  • Derive design guidelines from early analysis
  • Anticipate silicon, package and board structure

• Building a die model in a single step based on use-case for power integrity
  • Parametric models to enable multiple uses-cases from a single model

• Automation from design databases to model & simulation:
  • Use any data available from die design flow for die and package modeling
  • Reduce approximation and accuracy losses
  • Mapping, parametrization

• Accuracy vs runtime vs size/complexity of models

• Decoupling capacitor models compliance with application context
System Level Abstraction
System Power Delivery Network

Power Delivery Network (PDN): Supply system devices from voltage sources

- **Chip**
- **Package**
- **PCB**

**Decoupling Capacitors**
- **On Chip**
- **On Package**
- **On PCB**

**Capacitors**
- **Discrete Decoupling**
- **Low Inductance**
- **Bulk**

**Networks**
- **P/G**
- **Ball**

**Currents**
- **Very High Frequency**
- **High Frequency**
- **Middle Frequency**
- **Low Frequency**
- **Very Low Frequency**

**Voltage Regulator (VR)**

**Ground**

**Power**

**ΔI(t)**

VR = Voltage Regulator
System Level Modeling

- Any part of the PDN should be available as a model for accurate system level PI
  - Die part: CPM or equivalent model
  - Package part: RLCG spice model
  - Board part: RLCG spice model
  - Decoupling capacitor part: RLC spice model
  - Voltage regulator part: VRM

- System level models should enable power integrity analysis in Time and Frequency domains
Used PI Simulation Bench

- **Die CPM**
  - VDD
  - GND

- **On package decoupling**
  - VDD
  - GND

- **Bumps**
  - VDD
  - GND

- **Balls**
  - VDD
  - GND

- **On board decoupling**
  - VDD
  - GND

- **Board model**

- **VRM**
Power Integrity Analysis Outcome
System Level Power Integrity

• A system level Vdrop analysis taking into account the largest context
  • The full system model includes IC (CPM), package & board (S-parameters or RLCG), components (RLC, S-parameters) like capacitors, inductors and voltage regulator.
  • Simulation enables investigation into the effect of each component level phenomena on system level performance.
  • Package, board, die & component properties can be optimized to improve system behavior.

• Aim
  • Analyze supply network impedance and dynamic time domain behavior
  • Check voltage noise at IC level
  • Build implementation recommendations
  • Optimize package/board routing, decoupling capacitor values/location based on impedance/voltage targets and IC current needs
Power Integrity Analysis Result

- **Frequency domain**
  - PDN Impedance profile
  - Decoupling capacitor setup definition

- **Time domain**
  - Voltage drop map
  - Voltage noise at transistors or bumps
  - Voltage noise reduction proposal (layout and/or device behavior change)
System Level PI Analysis

Use-case pattern

IC

Vdrop

ANSYS RedHawk

Chip Power Model (CPM)

Component models
(Voltage regulator, capacitors...)

Package & Board models
(S-parameters, RLCG)

System simulation

Feedback loop

Mentor Graphics Eldo
Synopsys Hspice
Keysight ADS
ANSYS AEDT Circuit Design
...

Complete system level analysis:
IC + package + board + components
Impedance profile
Time domain voltage noise analysis
System Level PI Analysis

Use case pattern

Component models
(Voltage regulator, capacitors...)

IC
DB

Vdrop

ANSYS RedHawk

Package & Board models
(S-parameters, RLCG)

System level analysis (IC context):
IC + package + board + components
Time domain voltage noise analysis
Voltage Drop maps

IC
DB

Vdrop

Feedback loop

System level analysis (Package or Board contexts):
IC + package + board + components
Time domain voltage noise analysis
(Imedance profile)
Voltage Drop maps (static or dynamic)

Board
DB

Package & Board
Vdrop

ANSYS SIwave

Chip Power Model
(CPM)
Processing Unit PI – Result Example
ARM CPU

with WFI to Max Power to WFI Event

Current profile

Voltage noise
TCAM with Idle to Compare to Idle Event

System DC IR drop = 31.5mV
Package DC IR drop = 1.5mV

P2P (ignoring startup phase) = 30mV
P2P steady state = 9.2mV

P2P (ignoring startup phase) = 25mV
P2P steady state = 8.5mV

Possible decoupling cap for package

Impedance profile @ bump

Voltage noise

With decoupling cap
Without decoupling cap
With decoupling cap
Without decoupling cap
System Level PI Gains

Results extracted from some intermediate investigations on a ARM CPU integrated in a networking processor playing with on-die capacitors and package+board decoupling.
SERDES PI – Result Example
System Impedance Profile & voltage noise

Using PRBS and asynchronous start/stop of data lanes
Thanks

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